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EXAMINER	
TRUONG, LAN DAI T	
ART UNIT	**PAPER NUMBER**
2152	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/006,157	TARANOV, IGOR	
	Examiner	Art Unit	
	Lan-Dai Thi Truong	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is response to communications: application, filed on 12/10/2001; amendment filed 08/06/2007; claims 1-29 are pending; claims 1, 23 and 25 are amended

2. Applicant's arguments filed 08/06/2007have been fully considered, but new amended claims are moot in view of the new ground(s) of rejection.

Response to arguments

3. In response to applicant's argument to claims 1, 23 and 25 with respect to the network interface of the Tavana is a hardware component while the I/O completion port in claim 1 is a software is not persuasive; accordance to the definition of "the I/O completion port" in the specification, see (specification page 15, [0040]). Applicant discloses test packet sequencer comprises numbers of layers i.e. socket layer, test control layer and command layer wherein each layer deploys one I/O completion port to provide it's functionality. Tavana clearly discloses a system for time-stamping a data packets associated with data network allows a software application to determine the precise time that packets ware transmitted to or received from network. In Tavana's system, each station includes test application software and several layers of intermediate software, see (figure 1, items 18:1, 20:1; [0002]; [0003]). The test packets are generated and stamped departure times by the test application software and then sent into a network through the several layers of intermediate software for this reasons software I/O

completion ports should be included in the Tavana's system to support for software application and the several layers of intermediate software to implement their functionalities

4. Regarding applicant's arguments to claims 1, 23 and 25 with respect to the cited references do not disclose claimed feature of "the I/O completion port" implemented in the operating system running on a computer" are not persuasive. According to definition of "the I/O completion port" disclosed in the Specification, see (specification page 15, [0040]), Applicant discloses test packet sequencer comprises numbers of layers i.e. socket layer, test control layer and command layer wherein each layer deploys one I/O completion port to provide it's functionality. While Tavana discloses a network comprises communication between two stations (12, 14), see figure 1. Inherently processor and its I/O completion port included in those stations so steps of generating test packets, time-stamp test packets, dispatching test packet, calculating and determining transmitting delay time for those packet can be implemented, see (figure 1, items 18:1, 20:1; [0002]; [0003]).

IDS objections

Listing of references in the specification, see (page 10, lines 5-7) is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim rejections-35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 23 and 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which, such as, "measuring departure time/ and return time of each of the test packets using the I/O complete port" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no information demonstrates implementation of measuring departure time/ and return time of the test packets by the I/O in the specification. The appropriate correction is requested.

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 19, 21-23 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana et al. (U.S. 2002/0024973) in view of Lord et al. (U.S. 6,108,447)

Regarding claim 1:

Tavana discloses the invention substantially as claimed including method, which can be implemented in computer hardware or software code for dispatching bursts of packets onto a computer network, for dispatching a burst of test packets into a network, the method comprising:

Generating a plurality of test packets: (Tavana's system, The test packets are generated/ and stamped departure times by the test application software: figure 1, items 18:1, 20:1; [0002]; [0003]).

Measuring departure time of each of the test packets; measuring return time of each of the test packets: (In Tavana's system, test packets are generated/ and stamped departure time by the test application software and then sent into network through the several layers of intermediate software. Later the test packets travel back and received/ and stamped return time by the test application software. The application software then calculates the differences between the time-stag of the received/response packet and the time-tag of the sent packet to determine the round-trip propagation delay of the packet, see (figure 1, items 18:1, 20:1; [0002]; [0003]).

Forwarding to an I/O completion port a request that the test packets be dispatched, the I/O completion port implemented in an operating system running on a computer: (refer to definition of I/O completion port in the specification (page 15, [0040]). Applicant discloses test packet sequencer comprises numbers of layers i.e. socket layer, test control layer and command layer wherein each layer deploys one I/O completion port to provide it's functionality. In analogous art, Tavana clearly discloses a system for time-stamping a data packets associated

with a data network allows a software application to determine the precise time that packets ware transmitted to or received from network. In Tavana's system, each station includes test application software and several layers of intermediate software, see (figure 1, items 18:1, 20:1; [0002]; [0003]). The test packets are generated/ and stamped departure time by the test application software and then sent into network through the several layers of intermediate software. Later the test packets travel back and received/ and stamped return time by the test application software. Inherently, claimed I/O completion ports should be included in the Tavana's system to support for software application and the several layers of intermediate software communications and implementing their functionalities)

Dispatching the test packets onto the network using the I/O completion port: (as similar to rejection disclosed above, the I/O completion port inherently included in software application in order to be able to implement its' functionalities of generating test packets and sending them into network: (figure 1, items 18:1, 20:1; [0002]; [0003])

However, Tavana does not explicitly disclose using the I/O completion port measuring the time

In analogous art, Lord discloses technique of time stamping video sequence by following instructions received from "an application program interface" which shares functionality with "the I/O completion port" as claimed, see (abstract)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Lord's ideas of providing time-stamp instructions form an application software interface into Tavana's system in order to increase efficiencies for

communication system e.g. ability of capture real-time transmitting rate, see (column 1, lines 34-44)

Regarding claim 23:

This claim is rejected under rationale of claim 1

Regarding claim 19:

In addition to rejection in claim 1, Tavana- Lord further discloses Ethernet packets: (Tavana: [0041])

Regarding claim 21:

In addition to rejection in claim 1, Tavana- Lord further discloses receiving returning dispatched test packets after they have traversed a path in the network and time stamping notifications that the packets have been received: (Tavana: abstract, lines 1-13; figure 1; [0002])

Regarding claim 22:

Those claims are rejected under rationale of claim 1

Claim 2 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana- Lord in view of VanDervort (U.S 5,812,528)

Regarding claim 2:

Tavana- Lord discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the packets are forwarded to the I/O completion port asynchronously

However, VanDervort discloses a method of measuring "test cell" which is equivalent to "test packets" round trip time within an "ATM communication network " which is shared functionality with "forwarding to the I/O completion port asynchronously"(abstract: lines 1-16; column 1, lines 23-29)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine VanDervort's ideas of rounding of test cells in an asynchronous transfer mode with Tavana- Lord's system in order to provide flexibility of network configuration and implementation, see (VanDervort: column 2, lines)

Claims 3 and 8-9 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana- Lord in view of McKee et al. (U.S. 5,477,531)

Regarding claim 3

Tavana- Lord discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein forwarding the test packets to the I/O completion port is performed by a user mode thread during a single time slice; before forwarding the test packets, terminating the current time slice for the user thread; and forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread

However, McKee discloses a plurality of test packet in one burst are in the same "duration" which is equivalent to 'time slice." McKee also discloses one burst of a plurality of test packets has subsided before the next burst is sent, this process is shared functionality with "forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread": McKee: column 8, lines 40-42; column 9, lines 23-25)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine McKee's ideas of using single time slice to process test packet with Tavana- Lord's system in order to send out sequences of test packets to the target station, see (McKee: column 4, lines 8-12)

Regarding claim 8:

In addition to rejection in claim 3, Tavana- Lord - McKee further discloses returning test packet with time-stamp: (Tavana: [0002])

Regarding claim 9:

This claim is rejected under rationale of claims 3 and 8

Claim 17 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Lord -McKee in view of Williamsom, JR. et al. (U.S. 2003/0084388)

Regarding claim 17:

Tavana- Lord - McKee discloses the invention substantially as disclosed in claim 3, but does not explicitly teach network cards

In analogous art, Williamsom discloses test ports integrated with the card: ([0060]; [0007])

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Williamsom's ideas of using the network card with Tavana-Lord - McKee's system in order to provide convenient/efficiency for test system

Claims 4-7 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Lord -McKee in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claims 4-7:

Tavana- Lord - McKee discloses the invention substantially as disclosed in claim 3, but does not explicitly teach user mode

In analogous art, Madhavapeddi teach user-mode: (column 6, lines 64-67)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets

transmissions with Tavana- Lord - McKee's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

Claim 10 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Lord -McKee in view of Zhang et al. (U.S. 5,535,193)

Regarding claim 10:

Tavana- Lord -McKee discloses the invention substantially as disclosed in claim 9, but does not explicitly teach counter

In analogous art, Zhang discloses time-stamp counter, see (column 8, lines 29-35)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Zhang's ideas of using time-stamp counter with Tavana- Lord - McKee's system in order to provide an efficient transmitting packets timing measuring system, see (Zhang: abstract)

Claim 11 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Lord - McKee further in view of Johnson, Jr. (U.S. 5,640,504)

Regarding claim 11:

Tavana- Lord - McKee discloses the invention substantially as disclosed in claim 9, but does not explicitly teach maintaining a private heap for packet data, wherein the private heap is accessible to the user mode thread

However, Johnson discloses method of storing "the receiving information" which is equivalent to "returned test packet" into heap, see (Johnson: column 2, lines 12-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson's ideas of using heap for storing test packets with

Tavana- Lord - McKee's system in order to routing information see (Johnson: column 2, lines 12-15)

Claims 12-16 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana- Lord - McKee -Johnson Jr. in view of Garber et al. (U.S. 5,699,539)

Regarding claims 12-14:

Tavana- Lord - McKee -Johnson discloses the invention substantially as disclosed in claim 11, but does not explicitly teach wherein the private heap comprises standard-size allocation units for storing packets; wherein the standard-size allocation units are of an operating system memory page size; wherein the standard-size allocation units are 4096 bytes

However, Garber discloses a heap comprises allocation units for storing data. The allocation unit has size of 4096 bytes, see (Garber: column 1, lines 60-67; column 2, lines 48-54)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of using heap comprise 4096 bytes allocation units with Tavana- Lord - McKee -Johnson's system in order to provide compressing page, see (Garber: column 2, lines 48-54)

Regarding claims 15-16:

Tavana - Lord - McKee -Johnson discloses the invention substantially as disclosed in claim 11, but does not explicitly teach assigning a larger than default process working set size to the user mode thread; wherein the process working set size exceeds 8 Mbytes.

However, Garber discloses computer system with working set standard size of 8 Mbytes can take care process working set size of 16 Mbytes, see (Garber: column 1, lines 45-50)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of assigning a larger than default process working set size to the user mode thread with Tavana - Lord - McKee -Johnson's system in order to compress data, see (Garber: abstract, lines 1-27)

Claims 18 and 24 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana- Lord further in view of Ranmanathan et al. (U.S 6,076,113)

Regarding claims 18 and 24:

Tavana- Lord discloses the invention substantially as disclosed in claims 1 and 23, but does not explicitly teach wherein generating the test packets comprises generating a plurality of equal-sized test packets

However, Ranmanathan discloses equal size packets to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Ranmanathan's ideas of using equal size packets with Tavana-Lord's system in order to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Claim 20 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Lord -Ranmanathan in view of Crayford et al. (U.S. 6,016,308)

Regarding claim 20:

Tavana- Lord -Ranmanathan discloses the invention substantially as disclosed in claim 18, but does not explicitly teach wherein each of the test packets has a size in the range of 46 bytes to 1500 bytes

However, Crayford discloses Ethernet standards packet size is in range of 46 bytes to 1500 bytes, see (Crayford: column 2, lines 6-30)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Crayford's ideas of using packet size in range of 46 bytes to 1548 bytes with Tavana- Lord -Ranmanathan's system in order to indicate a standard frame of data to be sent over the network, see (Crayford: column 2, lines 1-30)

Claims 27-28 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana- Lord in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claims 27-28:

Tavana- Lord discloses the invention substantially as disclosed in claims 1 and 23, but does not explicitly teach kernel mode

In analogous art, Madhavapeddi discloses kernel mode for packets transmissions: column 6, lines 1-67; column 7, lines 47-52)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets transmissions with Tavana- Lord's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

Claims 25-26 are rejected under 35 U.S.C 103(a) as being un-patentable over Clark (U.S. 6,075,773) in view of Tavana et al. (U.S. 2002/0024973) and further in view of Lord et al. (U.S. 6,108,447)

Regarding claim 25:

Tavana discloses the invention substantially as claimed including method, which can be implemented in computer hardware or software code for dispatching bursts of packets onto a computer network, the apparatus comprising:

A computer processor: (Clark discloses a packet generating Ethernet testing device includes "a microprocessor" which shares functionality with " computer processor" as claimed: abstract)

A network interface: (Clark discloses "media interface" which shares functionality with "network interface" as claimed: abstract)

A program memory accessible to the processor, the program memory comprising test packet sequencer software comprising series of instructions executable by the processor under control of an operating system, the instructions, if executed by the processor, causing the processor to generating a plurality of test packets: (in Clark's system, "microprocessor" which shares functionality with "computer processor" as claimed, "packet memory" which shares functionality with "program memory" as claimed are connected/ and interoperate together in order to generate test packets; executable instruction inherently included in microprocessor of the Clark: abstract)

However, Clark does not explicitly disclose test packet sequencer software and first I/O completion port

In analogous art, Tavana clearly discloses a system for time-stamping a data packets associated with a date network allows a software application to determine the precise time that packets ware transmitted to or received from network. In Tavana's system, each station includes "test application software" which shares functionality with "test packet sequencer software" and

several layers of intermediate software, see (figure 1, items 18:1, 20:1; [0002]; [0003]). The test packets are generated/ and stamped departure times by the test application software and then sent into network through the several layers of intermediate software. Later the test packets travel back and received/ and stamped return time by the test application software. Refer to the definition of "the I/O completion port" in the specification, see (specification page 15, [0040]). Applicant discloses test packet sequencer comprises numbers of layers i.e. socket layer, test control layer and command layer wherein each layer deploys one I/O completion port to provide it's functionality; so inherently claimed I/O completion ports should be included in the Tavana's system to support for software application and the several layers of intermediate software communications and implementing their functionalities: [0002]; [0003])

Forward to the first I/O completion port a request that the test packets be dispatched, the first I/O completion port; the first I/O completion port implemented in the operating system running on the processor: (as similar to the rejections addressed above, the I/O completion port inherently included in Tavana's work station (12, 14) for supporting communications of numbers layers (i.e. 116, 114, 106, 108 and 102). In Tavana's system, the I/O completion port inherently supports software application implements it's functionalities of generating test packets and dispatching them into network)

Dispatching the test packets onto the network by way of the network interface using the I/O completion port: (In Tavana's system, the I/O completion port inherently included in software application in order to be able to implement its' functionalities such as generating test packets and sending them into network through numbers of layers of intermediate software and "PHY 24:2" which also shares functionality with "the network interface" as claimed and

inherently includes the I/O completion port for implementing test packets dispatching into network: figure 1, items 18:1, 20:1; [0002]; [0003])

Measuring departure time of each of the test packets; measuring return time of each of the test packets: (In Tavana's system, test packets are generated/ and stamped departure time by the test application software and then being sent into network through the several layers of intermediate software. Later the test packets travel back and received/ and stamped return time by the test application software. The application software then calculates the differences between the time-stag of the received/response packet and the time-tag of the sent packet to determine the round-trip propagation delay of the packet, see (figure 1, items 18:1, 20:1; [0002]; [0003])

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Tavana's ideas of measuring packet traveling times into Clark's system in order to be able to determine delay packet transmitting times for communication speed improvement purpose, see (Tavana: [0003]-[0006])

However Clark- Tavana does not explicitly disclose using the I/O completion port for time measuring purpose

In analogous art, Lord discloses technique of time stamping video sequence by following instructions received from "an application program interface" which shares functionality with "the I/O completion port" as claimed, see (abstract)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Lord's ideas of providing time-stamp instructions form an application software interface into Clark- Tavana's system in order to increase efficiencies for

communication system e.g. ability of capture real-time transmitting rate, see (column 1, lines 34-44)

Regarding claim 26:

In addition to rejection in claim 25, Clark-Tavana-Lord further discloses the test packet sequencer software comprises a test controller layer associated with a I/O completion port and command: (as similar to discussions addressed above, In Tavana's system, the I/O completion port/ and commands inherently included "in software application" which shares functionality with "the test packet sequencer software" as claimed in order to be able to implement its' functionalities such as generating test packets and sending them into network through numbers of layers of intermediate software and "PHY 24:2" which also shares functionality with "the network interface" as claimed: figure 1, items 18:1, 20:1; [0002]; [0003])

Claim 29 is rejected under 35 U.S.C 103(a) as being un-patentable over Clark-Tavana-Lord in view of Madhavapeddi et al. (U.S. 6,975,656)

Regarding claim 29:

Clark-Tavana-Lord discloses the invention substantially as disclosed in claims 25, but does not explicitly teach kernel mode

In analogous art, Madhavapeddi discloses kernel mode for packets transmissions: column 6, lines 1-67; column 7, lines 47-52)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Madhavapeddi's ideas of using kernel mode for packets transmissions with Clark-Tavana-Lord's system in order to provide efficiency/ high-resolution for data transmission network, see (Madhavapeddi: abstract)

The prior arts made of records and not relied upon are considered pertinent to applicant's disclosure. The following patents and publications are cited to further show the state of the art with respect to "Methods and apparatus for placement of test packets into data communication network": 20010021981; 6163805; 5913073; 4682330; 20020194545; 6502051; 6084944; 7171464 (kernel mode); 6034948 (mode)

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusions

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lan-Dai Thi Truong whose telephone number is 571-272-7959. The examiner can normally be reached on Monday- Friday from 8:30am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob A. Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

10/11/2007

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER

10/14/7